WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a body region of a first conductivity type formed in a semiconductor substrate;

a plurality of trench gates extending through the body region;

a plurality of first semiconductor regions of a second conductivity type that is different from the first conductivity type, the first semiconductor regions having a first depth as measured from a surface of the body region and sandwiching the trench gates via the gate-insulating films; and

a plurality of second semiconductor regions of the second conductivity type having a second depth as measured from the surface of the body region that is less than the first depth,

wherein the second semiconductor regions connect the plurality of first semiconductor regions spaced apart from one another.

2. A semiconductor device according to claim 1, wherein at least a portion of the first semiconductor regions sandwich the trench gates via the gate-insulating film.

3. A semiconductor device according to claim 2, wherein the first semiconductor regions are formed along

the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-like configuration.

4. A semiconductor device according to claim 1, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-like configuration.

5. A semiconductor device according to claim 1, further comprising a wiring member connected to at least one of the plurality of trench gates.

6. A semiconductor device according to claim 2, further comprising a wiring member connected to at least one of the plurality of trench gates.

7. A semiconductor device according to claim 3, further comprising a wiring member connected to at least one of the plurality of trench gates.

8. A semiconductor device according to claim 4, further comprising a wiring member connected to at least one of the plurality of trench gates.

9. A semiconductor device according to claim 1,

further comprising a wiring member connected to the body region and to the second semiconductor region.

10. A semiconductor device according to claim 2, further comprising a wiring member connected to the body region and to the second semiconductor region.

11. A semiconductor device according to claim 3, further comprising a wiring member connected to the body region and to the second semiconductor region.

12. A semiconductor device according to claim 4, further comprising a wiring member connected to the body region and to the second semiconductor region.

13. A process for producing a semiconductor device comprising:

forming a body region of a first conductivity type in a semiconductor substrate;

forming a plurality of trench gates extending through the body region;

forming a plurality of first semiconductor regions of a second conductivity type that is different from the first conductivity type, the first semiconductor regions having a first depth as measured from a surface of the body region and sandwiching the trench gates via gate-insulating films;

forming a plurality of second semiconductor regions

of the second conductivity type having a second depth as measured from the surface of the body region that is less than the first depth; and

connecting the plurality of first semiconductor regions spaced apart from one another by the second semiconductor regions.

14. A process according to claim 13, wherein at least a portion of the first semiconductor regions sandwich the trench gates via the gate-insulating film.

15. A process according to claim 14, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-like configuration.

16. A process according to claim 13, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-like configuration.

17. A process according to claim 13, further comprising:

forming a wiring member connected to at least one of the plurality of trench gates.

18. A process according to claim 13, further comprising:

forming a wiring member connected to the body region and to the second semiconductor region.